

CLAIMS

1 ✓ 1. A controller for a random access memory comprises:
2 an address and command queue that holds memory
3 references from a plurality of microcontrol functional units;
4 a first read/write queue that holds memory reference
5 from a computer bus;
6 a second read/write queue that holds memory references
7 from a core processor; and
8 control logic including an arbiter that detects the
9 fullness of each of the queues and a status of outstanding memory
10 reference to select a memory reference from one of the queues.

1 ✓ 2. The controller of claim 1 wherein the control logic
2 further selects one of the queues to provide a next memory
3 references based on a programmable value stored in a priority
4 service control register.

1 ✓ 3. The controller of claim 1 wherein the address and
2 command queue comprises:
3 a high priority queue that holds memory references from
4 high priority tasks.

1 ○ 4. The controller of claim 1 wherein the address and
2 command queue comprises:
3 an even bank queue;
4 an odd bank queue; and
5 wherein a microengine sorts memory references into odd
6 bank and even bank references.

1 ○ 5. The controller of claim 1 wherein the address and
2 command queue comprises:

3 an order queue and wherein controller examines an
4 optimized memory reference bit and if set, causes incoming
5 reference requests to be sorted into either the even bank queue
6 or the odd bank queue.

1 6. The controller of claim 5 wherein the address and
2 command queue comprises:
3 an order queue; and
4 wherein if the memory reference request does not have a
5 memory optimization bit set, the memory reference is stored in
6 the order queue.

1 7. The controller of claim 1 wherein the address and
2 command queue is implemented in a single memory structure and
3 comprises:
4 an order queue for storing memory references;
5 an even bank queue for storing memory references;
6 an odd bank queue for storing memory references;
7 a high priority queue for storing memory references;
8 and
9 with the memory structure being segmented into four
10 different queue regions, each region having its own head and tail
11 pointer.

1 8. The controller of claim 7 wherein the address and
2 command queue further comprises:
3 an insert queue control and a remove queue arbitration
4 logic to control insert and removal of memory references from the
5 queues.

1 9. The controller of claim 1 further comprising:
2 a command controller and address generator that is

3 responsive to an address from a selected memory reference from
4 one said queues, to produce addresses and commands to control a
5 memory interface.

1 ✓ 10. The controller of claim 9 further comprising:
2 a memory interface responsive to generated addresses
3 and commands to produce memory control signals.

1 ✓ 11. The controller of claim 1 wherein the control logic is
2 responsive to a chaining bit that when set allows for special
3 handling of contiguous memory references.

1 12. The controller of claim 1 wherein assertion of the
2 chain bit will control the arbiter to have the arbiter select the
3 functional unit which previously requested that bus because
4 setting of the chain bit indicates that the microengine issued a
5 chain request.

1 13. The controller of claim 1 wherein the control logic is
2 responsive to an optimized memory bit and a chaining bit, and
3 wherein assertion of the chaining bit will control the arbiter
4 when the optimized memory bit is also set to maintain the memory
5 references from a current queue.

1 ✓ 14. The controller of claim 1 wherein the arbiter has an
2 arbitration policy that favors chained microengine memory
3 references.

1 ✓ 15. The controller of claim 14 wherein the arbiter has an
2 arbitration policy that services chained requests until the chain
3 bit is cleared.

1 ✓ 16. The controller of claim 1 wherein the arbiter has an
2 arbitration policy that starts by examining for chained
3 microengine memory reference requests.

1 ✓ 17. The controller of claim 16 wherein the arbitration
2 policy enables chained memory requests to be serviced completely.

1 ✓ 18. The controller of claim 16 wherein when the chain bit
2 is set, the arbitration engine services the same queue again
3 until the chain bit is cleared.